

SoC Design Team Lead —ARM Based Micro-controller

BareMetal Systems · Engineering · SoC Design

We're scaling our ARM-based micro-controller SoC program from first architecture through first silicon, and we need someone who can lead that journey end to end — setting the architecture direction, unblocking the team's toughest integration problems, and owning MPW execution from readiness review to tape-out.

About BareMetal Systems

BareMetal Systems builds ARM-based micro-controller SoCs for embedded and real-time applications. Our engineers work across the full stack — from computer architecture and RTL integration through FPGA prototyping and silicon bring-up — and we care as much about getting the architecture right on day one as we do about shipping clean silicon.

About the Role

As SoC Design Team Lead, you'll own the architecture direction for our ARM-based micro-controller SoCs and lead the engineers translating that architecture into RTL, FPGA prototypes, and tape-out-ready silicon. Twelve months in, you'll have driven at least one MPW shuttle from architecture freeze through clean handoff, built a team that can move confidently from whiteboard architecture discussions to RTL integration details, and established the review processes that catch architectural and integration issues before they become late-cycle bugs.

What You'll Do

- Define and own ARM-based micro-controller SoC architecture — CPU subsystem integration, memory map planning, bus architecture, interrupt structure, clocking, reset strategy, and peripheral interconnect
- Lead performance, area, power, and cost trade-off analysis during early architecture exploration, and make the final calls when trade-offs conflict
- Guide the team integrating ARM processor cores, standard IPs, custom accelerators, memory interfaces, and peripheral blocks into a cohesive SoC platform
- Drive MPW shuttle planning and execution — design readiness reviews, IP/package selection, foundry collateral coordination, sign-off checklist ownership, and silicon bring-up preparation
- Mentor design engineers on computer architecture fundamentals and RTL integration practice, and review their microarchitecture and design specifications
- Be the escalation point for pre-silicon debug and post-silicon validation when the root cause is architectural or integration-related
- Represent the design team in cross-functional planning with firmware, verification, physical design, DFT, and applications teams to keep architecture decisions implementation-feasible

Computer Architecture — Why It Matters Here

This is fundamentally an architecture leadership role. You'll be the person the team turns to when a design decision needs a computer-architecture answer: how a cache or memory hierarchy choice affects real-world performance, how an AMBA-based interconnect topology should be structured for a given bandwidth and latency budget, where a pipelining or interrupt-handling decision will bite us six months from now. Strong, current computer architecture judgment — not just RTL fluency — is what this role is built around.

What We're Looking For — Required

- 5+ years of experience in SoC design, RTL integration, or micro-controller architecture, including some experience leading or mentoring other engineers
- Deep, applied understanding of computer architecture: pipelining, memory hierarchy, AMBA-based interconnects (AHB/APB/AXI), interrupts and exception handling, cache and memory system behavior, and performance bottleneck analysis
- Hands-on experience with ARM-based system design, especially Cortex-M or similar embedded processor integration
- Track record of taking a micro-controller SoC through an MPW shuttle — design readiness reviews, sign-off, and tape-out handoff
- Solid RTL design and integration skills in Verilog or SystemVerilog, and comfort reviewing others' RTL and architecture specs
- Experience with FPGA prototyping (Xilinx, Intel, or Lattice) for SoC or subsystem validation
- Strong cross-functional collaboration skills — this role interfaces constantly with architecture, verification, physical design, DFT, firmware, and applications teams

Preferred (Nice to Have)

- Experience owning ARM micro-controller subsystem design end to end, including timers, watchdogs, GPIO, UART, SPI, I2C, PWM, ADC, or motor-control-oriented peripherals
- Familiarity with TrustZone, secure boot, DMA, power management, low-power modes, and embedded debug/trace features
- Exposure to SRAM/compiler memories, ROM integration, eFuse/OTP concepts, and boot architecture
- Understanding of DFT considerations, scan integration, MBIST, and production test implications
- Experience with UPF/low-power intent, STA-aware design considerations, and physical implementation trade-offs
- Post-silicon bring-up, lab validation, and firmware-assisted debug leadership experience
- Scripting with Python, Tcl, or shell to automate design flows